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Term: L2 and (NIC or (network adj1 interface adj1 card)).ab.

Display: 10 **Documents in Display Format:** KWIC **Starting with Number** 1

Generate: ○ **Hit List** ◉ **Hit Count** ○ **Side by Side** ○ **Image**

Search Clear Interrupt

Search History

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L3	L2 and (NIC or (network adj1 interface adj1 card)).ab.	86	L3
L2	709/$.ccls.	17245	L2
L1	6070253.pn.	1	L1

END OF SEARCH HISTORY

L3/82,
NIC
DMA

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N | C

US005778180A

United States Patent [19]

Gentry et al.

[11] Patent Number: 5,778,180

[45] Date of Patent: Jul. 7, 1998

[54] **MECHANISM FOR REDUCING DATA COPYING OVERHEAD IN PROTECTED MEMORY OPERATING SYSTEMS**

[75] Inventors: **Denton E. Gentry**, Palo Alto; **Rasoul M. Oskouy**, Fremont, both of Calif.

[73] Assignee: **Sun Microsystems, Inc.**, Mountain View, Calif.

[21] Appl. No.: 554,608

[22] Filed: Nov. 6, 1995

[51] Int. Cl.[6] G06F 13/14

[52] U.S. Cl. 395/200.42; 395/842

[58] Field of Search 395/200.2, 250, 395/200.07, 842, 846, 848, 200.42; 370/412, 392, 395

[56] **References Cited**

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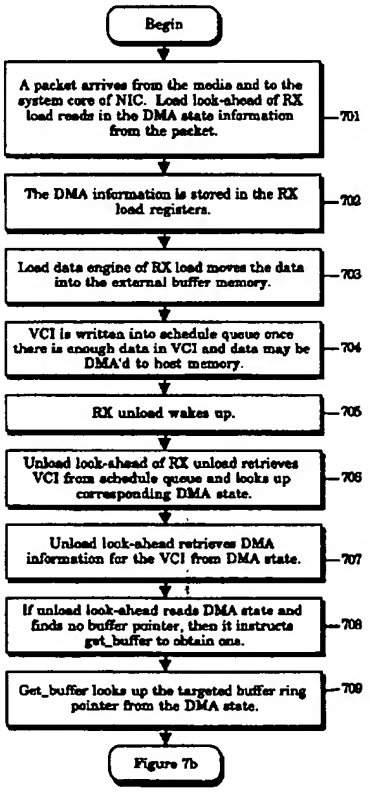
5,633,867	5/1997	Ben-Nun	370/399
5,640,399	6/1997	Rostoker	370/392
5,666,514	9/1997	Cheriton	711/144

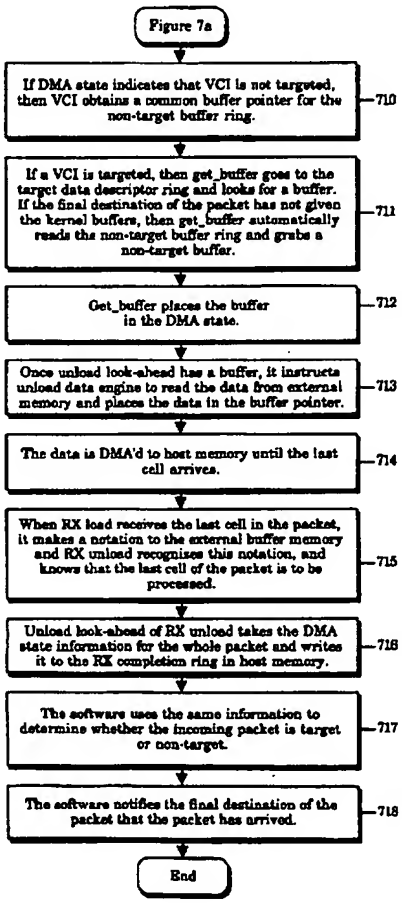
Primary Examiner—Tod R. Swann
Assistant Examiner—Christopher Chow
Attorney, Agent, or Firm—Blakely Sokoloff Taylor & Zafman

[57] **ABSTRACT**

A method and an apparatus for reducing data copying overhead associated with protected memory operating systems. In an ATM (Asynchronous Transfer Method) network, the present invention's NIC (network interface circuit) demultiplexes the information in the header of the incoming packet and routes the packet directly to its final destination using the present invention's concept of targeted buffer rings. Thus, instead of having the packet be DMA'd to a buffer in a descriptor ring in the kernel, it may be routed directly to the buffer ring of the destination process.

29 Claims, 13 Drawing Sheets





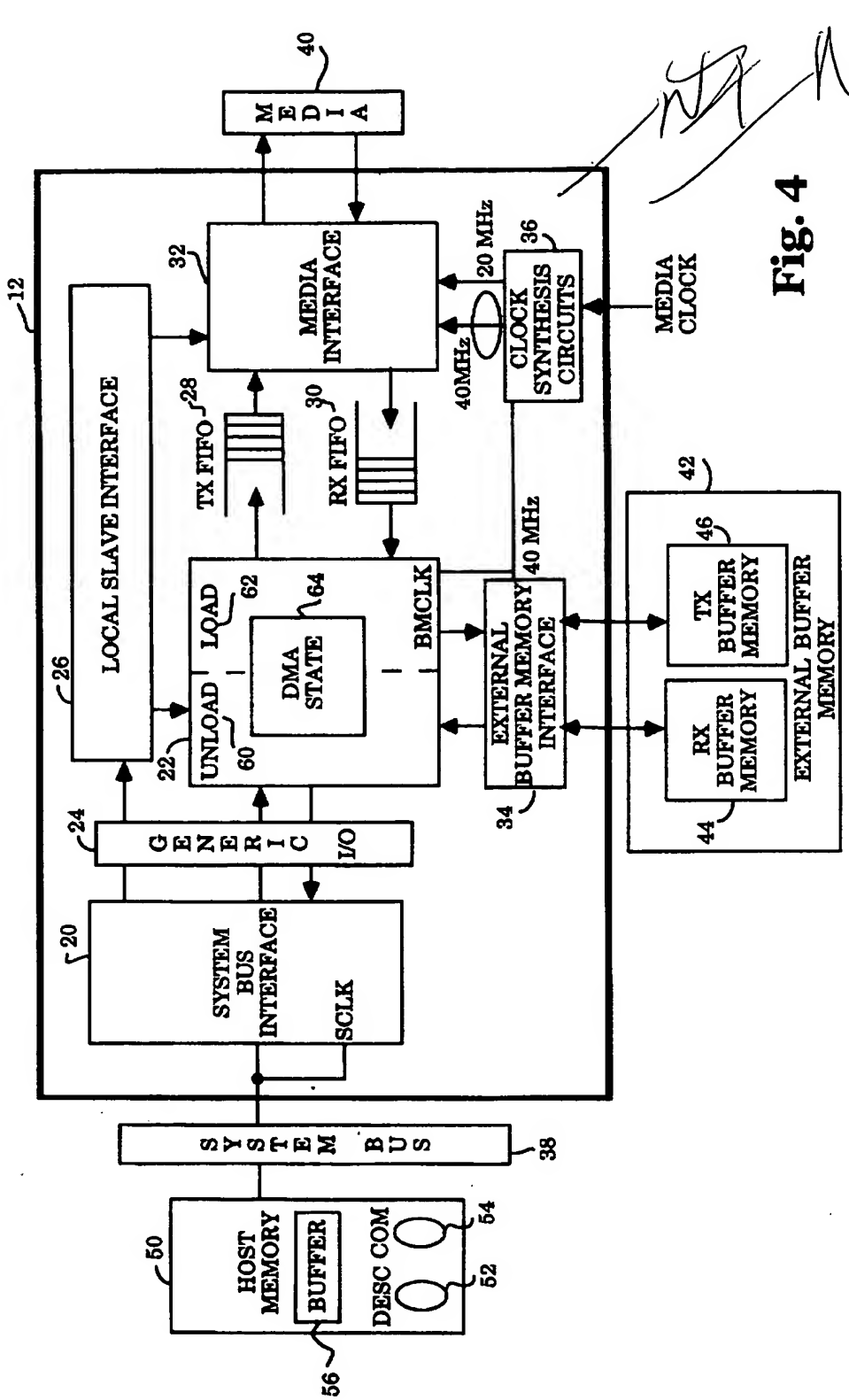

NIC
40
MEDIA
12
32
MEDIA INTERFACE
20 MHz
36
CLOCK SYNTHESIS CIRCUITS
MEDIA CLOCK
40MHz
LOCAL SLAVE INTERFACE
28
TX FIFO
30
RX FIFO
42
46
TX BUFFER MEMORY
40 MHz
62
LOAD
64
DMA STATE
BMCLK
EXTERNAL BUFFER MEMORY INTERFACE
RX BUFFER MEMORY
EXTERNAL BUFFER MEMORY
26
22
UNLOAD
60
34
44
24
GENERIC I/O
20
SYSTEM BUS INTERFACE
SCLK
SYSTEM BUS
38
50
HOST MEMORY
BUFFER
DESC COM
54
52
56

Fig. 4

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L3: Entry 82 of 86 File: USPT Jul 7, 1998

DOCUMENT-IDENTIFIER: US 5778180 A
TITLE: Mechanism for reducing data copying overhead in protected memory operating systems

NIC

Abstract Text (1):
A method and an apparatus for reducing data copying overhead associated with protected memory operating systems. In an ATM (Asynchronous Transfer Method) network, the present invention's NIC (network interface circuit) demultiplexes the information in the header of the incoming packet and routes the packet directly to its final destination using the present invention's concept of targeted buffer rings. Thus, instead of having the packet be DMA'd to a buffer in a descriptor ring in the kernel, it may be routed directly to the buffer ring of the destination process.

Current US Original Classification (1):
709/212

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BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates the method and apparatus of a traditional approach to data access for protected memory operating systems.

FIG. 2 illustrates the general steps followed by an exemplary implementation of the prior art method and apparatus (references are made to elements illustrated in FIG. 1).

FIG. 3 illustrates an exemplary computer system network incorporating the ATM network interface circuit which utilizes the method and apparatus of data access of the present invention.

FIG. 4 is a simplified system diagram illustrating the architecture of the ATM NIC of FIG. 3.

FIG. 5 is a general overview of the preferred data structure of the host memory used for data reception.

FIG. 6 illustrates the receive RX unload, the DMA state and the RX load of system core illustrated in FIG. 4.

FIGS. 7*a* and 7*b* are flow diagrams illustrating the general steps followed by an exemplary implementation of the present invention.

FIG. 8 illustrates an exemplary format for the DMA state of the receive block.

FIG. 9 illustrates an exemplary application of the present invention of transferring incoming packets directly to its destination.

FIG. 10 is a flow diagram illustrating the general steps followed by an exemplary implementation of the present invention as illustrated in FIG. 9.

FIG. 11 illustrates an exemplary implementation of the present invention under an abort condition.

FIG. 12 is a flow diagram illustrating the general steps followed by an exemplary implementation of the present invention under an abort condition.

DETAILED DESCRIPTION OF THE INVENTION

A method and an apparatus for data transfer reducing the data copying overhead associated with protected memory operating systems. In an ATM (Asynchronous Transfer Method) network, the present invention's NIC (network interface circuit) demultiplexes the information in the header of the incoming packet and routes the packet directly to its final destination using the present invention's concept of targeted buffer rings.

With the present invention, the software may select a more efficient routing of the packet to its final destination. Addressing is performed at several different levels. More specifically, at the ATM layer there is a VCI in every cell header. The router used as the VCI to determine which targeted buffer to read or write by DMA. Inside the packet is another set of headers with another set of address, typically Internet Protocol (IP) addresses. The router never looks at the IP address. Since there are multiple VCI's coming into a host, there can be multiple targeted buffer rings and multiple user processes can receive their data with no copying.

Thus, instead of having the packet be sent to a buffer by DMA corresponding to a descriptor on the kernel's descriptor ring, the software may route the packet to a different buffer ring. The software may be used to designate in advance that a particular buffer ring in the kernel points to buffers already in the final destination. Thus, when a packet arrives, the router selects a descriptor pointing to a buffer already in the packet's final destination, writes the data into that buffer by DMA and notifies the kernel that the packet has arrived. The kernel then looks up the header of the packet and tells the final destination that the packet is in the final destination. The method and apparatus of the present invention therefore reduces the data copying overhead associated with protected memory operating systems and increases overall system performance.

FIG. 3 illustrates an exemplary computer system network incorporating a ATM network interface circuit (NIC) which utilizes the method and apparatus for reducing data copying overhead of the present invention. The computer system network **10** includes host computer systems (not shown) which incorporate one or more of the ATM network interface circuits (NICs) **12**. The NICs **12** are coupled to a public ATM switch **16** through a local ATM switch **14** to enable asynchronous transfer of data between host computer systems coupled to the network **10**. Alternately, the NICs **12** can be coupled directly to the public ATM switch **16**. As shown in FIG. 3, the computer system network **10** may also include computer systems which incorporate the use of a Local Area Network ("LAN") emulation **15** which serves as a gateway for connecting other networks such as Ethernet or token ring networks **17** which utilize the ATM network as a supporting framework.

FIG. 4 is a simplified system diagram illustrating the architecture of the ATM NIC **12** of FIG. 3. The ATM NIC **12** interfaces the host computer system coupled through system bus **38** to the network media **40** operating in accordance with the ATM protocol.

The ATM NIC **12** shown includes a System Bus interface **20**, a Generic Input/Output ("GIO") interface **24**, a System and ATM Layer Core **22**, a Local Slave interface **26**, an array of transmit (TX) FIFOS **28**, an array of receive (RX) FIFOS **30**, a Media interface **32**, an External Buffer Memory Interface **34** and clock synthesis circuit **36**.

Together, the elements **20–36** of network interface circuit **12** cooperate to asynchronously transfer data between the host computer and the other computers in the network through multiple, dynamically allocated channels in multiple bandwidth groups. Collectively, the elements of the network interface circuit **12** function as a multi-channel intelligent direct memory access (DMA) controller coupled to the System Bus **38** of the host computer system. In a preferred embodiment, multiple transmit and receive channels are serviced as virtual connections utilizing a full duplex 155/622 Mbps physical link. Multiple packets of data, subscribed to different channels over the System Bus **38** to the external buffer memory **42**, via the External Buffer Memory Interface **34**, are segmented by the System and ATM Layer Core **22** into transmit cells for transmission to the Media **40** through Media interface **32**.

The Core **22** also comprises reassembly logic to facilitate reassembly of the receive packets. The TX and RX FIFOS **28**, **30**, coupled between the Core **22** and the Media Interface **32**, are used to stage the transmit and receive cell payloads of the transmit and receive packets respectively. The Media Interface **32** transmits and receives cells to the Media **40** of the network, driven by clock signals provided by Clock Synthesis Circuit **36**. Preferably the Media, and therefore the Media interface **32**, conforms to the Universal Test and Operations Physical Interface for ATM ("UTOPIA") standard, as provided by the ATM Forum Ad Hoc specification. To conform to the UTOPIA specification, the clock synthesis circuit **36** provides either a clock signal of 20 MHz or 40 MHz to enable the Media interface **32** to support a byte stream at 20 MHz for 155 Mbps or a 16 bit stream at 40 MHz for a 622 Mbps data stream.

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Term: L1 and (peripheral adj3 (network adj1 interface adj1 card))

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L7	L1 and ((network adj1 interface adj1 card) adj3 NIC)	416	L7
L6	L1 and (((NIC) or (network adj1 interface adj1 card)) with peripheral$ with download$)	1	L6
L5	L1 and (((NIC) or (network adj1 interface adj1 card)) with peripheral$with download$)	0	L5
L4	L1 and (((NIC) or (network adj1 interface adj1 card)) with peripheral$)	82	L4
L3	6141705.pn.	1	L3
L2	L1 and (((NIC) or (network adj1 interface adj1 card)) with peripheral$).ab.	3	L2
L1	709/$.ccls.	17245	L1

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L8: Entry 16 of 18 File: USPT May 30, 2000

DOCUMENT-IDENTIFIER: US 6070253 A
TITLE: Computer diagnostic board that provides system monitoring and permits remote terminal access

Current US Cross Reference Classification (1):
709/223

CLAIMS:

17. The system management module of claim 15, wherein the peripheral devices include a network interface card, permitting direct connection between the system management module and a system network.

Previous Doc Next Doc Go to Doc#

US006070253A

United States Patent [19]

Tavallaei et al.

[11] Patent Number: 6,070,253

[45] Date of Patent: *May 30, 2000

[54] **COMPUTER DIAGNOSTIC BOARD THAT PROVIDES SYSTEM MONITORING AND PERMITS REMOTE TERMINAL ACCESS**

[75] Inventors: **Siamak Tavallaei**, Spring; **Joseph Peter Miller**; **Paul R. Culley**, both of Cypress, all of Tex.

[73] Assignee: **Compaq Computer Corporation**, Houston, Tex.

[*] Notice: This patent is subject to a terminal disclaimer.

[21] Appl. No.: **08/775,819**

[22] Filed: **Dec. 31, 1996**

[51] **Int. Cl.**[7] **H05K 10/00**; G06F 15/173

[52] **U.S. Cl.** **714/31**; 709/223

[58] **Field of Search** 395/200.53, 200.54, 395/183.01, 183.03, 183.07, 184.01; 709/223–224; 714/25, 27, 31, 47

[56] **References Cited**

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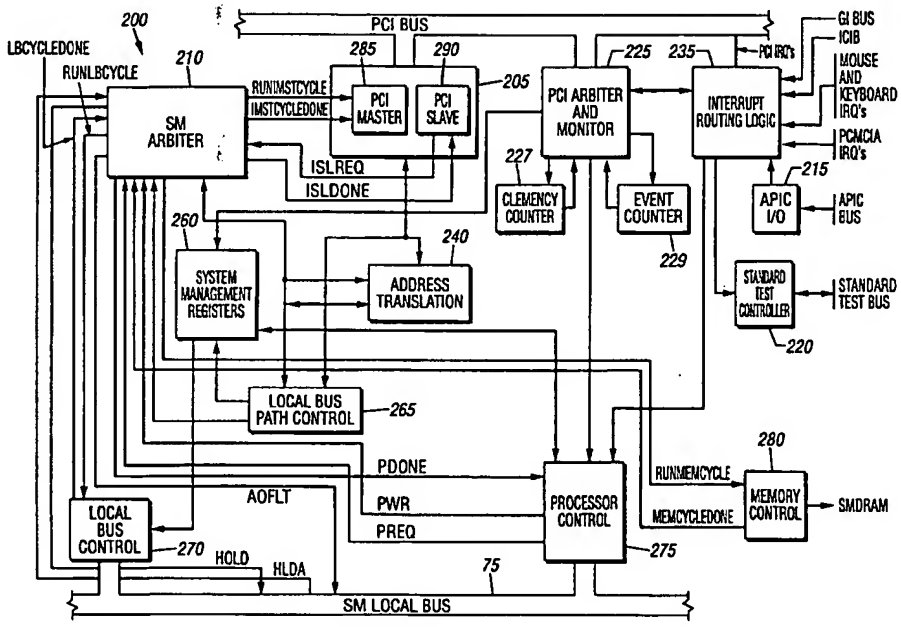
5,933,614	8/1999	Tavallaei et al.	710/129

Primary Examiner—Zarni Maung
Assistant Examiner—Andrew Caldwell
Attorney, Agent, or Firm—Conley, Rose & Tayon, P.C.; Michael F. Heim; Jonathan M. Harris

[57] **ABSTRACT**

A system management module (SMM) for a host server system includes a system management processor (SMP) connected to a system management local bus. The system management local bus connects to the system PCI bus through a system management central (SMC). The SMC includes the main arbitration unit for the PCI bus and also includes the arbiter for the system management local bus. The SMM includes a video controller and/or keyboard and mouse controller connected to the system management local bus to support remote consoling of the SMM. The video controller is further used for transmitting screen images to a remote computer system to facilitate system failure analysis. A plurality of system management remote units are provided for coupling to various components and busses within the host computer system. The system management remote units (SMR's) connect to the SMM via serial bus and permit the SMM to automatically monitor activities and operating conditions, including determining the source of interrupts on busses and detecting error conditions.

28 Claims, 10 Drawing Sheets



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L3	6141705.pn.	1	L3
L2	L1 and (((NIC) or (network adj1 interface adj1 card)) with peripheral$).ab.	3	L2
L1	709/$.ccls.	17245	L1

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Search Results - Record(s) 1 through 3 of 3 returned.

☐ 1. Document ID: US 6370599 B1

L2: Entry 1 of 3 File: USPT Apr 9, 2002

date N6

DOCUMENT-IDENTIFIER: US 6370599 B1
**** See image for Certificate of Correction ****
TITLE: System for ascertaining task off-load capabilities of a device and enabling selected capabilities and when needed selectively and dynamically requesting the device to perform the task

Abstract Text (1):
The present invention is directed to a method and computer program product for offloading specific processing tasks that would otherwise be performed in a computer system's processor and memory, to a peripheral device, or devices, that are connected to the computer. The computing task is then performed by the peripheral, thereby saving computer system resources for other computing tasks and increasing the overall computing efficiency of the computer system. In one preferred embodiment, the disclosed method is utilized in a layered network model, wherein computing tasks that are typically performed in network applications are instead offloaded to the network interface card (NIC) peripheral. An application executing on the computer system first queries the processing, or task offload capabilities of the NIC, and then selectively enables those capabilities that may be subsequently needed by the application. The specific processing capabilities of a NIC are made available by creating a task offload buffer data structure, which contains data indicative of the processing capabilities of the corresponding NIC. Once an application has discerned the capabilities of a particular NIC, it will selectively utilize any of the enabled task offload capabilities of the NIC by appending packet extension data to the network data packet that is forwarded to the NIC. The device driver of the NIC will review the data contained in the packet extension, and then cause the NIC to perform the specified operating task(s). This offloading of computing tasks on a per-packet basis allows an application to selectively offload tasks on a dynamic, as-needed basis. As such, applications executing on the computer system processor are able to offload tasks in instances where it is busy processing other computing tasks and processor overhead is high. Multiple tasks can also be offloaded in batches to a particular peripheral.

Current US Cross Reference Classification (1):
709/203

Current US Cross Reference Classification (2):
709/219

h e b b g e e e f e g ef b e

☐ 2. Document ID: US 6178462 B1

L2: Entry 2 of 3 File: USPT Jan 23, 2001

DOCUMENT-IDENTIFIER: US 6178462 B1
TITLE: Protocol for using a PCI interface for connecting networks

Abstract Text (1):
A system for coupling a local area network to a wide area network utilizes a PCI (Peripheral Component Interface) bus to couple a PCI interface to a PCI network interface card, which is coupled to the wide area network. The wide area network could be an asynchronous transfer mode network or a high bandwidth ethernet. If the PCI network interface card operates as a PCI master, then the PCI interface will operate as a PCI slave. If the PCI network interface card operates as a PCI slave, then the PCI interface of the invention will operate as a PCI master.

Current US Original Classification (1):
709/249

Current US Cross Reference Classification (1):
709/208

Current US Cross Reference Classification (2):
709/209

☐ 3. Document ID: US 6141705 A

L2: Entry 3 of 3 File: USPT Oct 31, 2000

Date NG

DOCUMENT-IDENTIFIER: US 6141705 A
**** See image for Certificate of Correction ****
TITLE: System for querying a peripheral device to determine its processing capabilities and then offloading specific processing tasks from a host to the peripheral device when needed

Abstract Text (1):
The present invention is directed to a method and computer program product for offloading specific processing tasks that would otherwise be performed in a computer system's processor and memory, to a peripheral device, or devices, that are connected to the computer. The computing task is then performed by the peripheral, thereby saving computer system resources for other computing tasks and increasing the overall computing efficiency of the computer system. In one preferred embodiment, the disclosed method is utilized in a layered network model, wherein computing tasks that are typically performed in network applications are instead offloaded to the network interface card (NIC) peripheral. An application executing on the computer system first queries the processing, or task offload capabilities of the NIC, and then selectively enables those capabilities that may be subsequently needed by the application. The specific processing capabilities of a NIC are made available by creating a task offload buffer data structure, which contains data indicative of the processing capabilities of the corresponding NIC.

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Once an application has discerned the capabilities of a particular NIC, it will selectively utilize any of the enabled task offload capabilities of the NIC by appending packet extension data to the network data packet that is forwarded to the NIC. The device driver of the NIC will review the data contained in the packet extension, and then cause the NIC to perform the specified operating task(s). This offloading of computing tasks on a per-packet basis allows an application to selectively offload tasks on a dynamic, as-needed basis. As such, applications executing on the computer system processor are able to offload tasks in instances where it is busy processing other computing tasks and processor overhead is high. Multiple tasks can also be offloaded in batches to a particular peripheral.

Current US Cross Reference Classification (1):
709/203

Current US Cross Reference Classification (2):
709/219

Current US Cross Reference Classification (3):
709/223

Term	Documents
NIC	3856
NICS	618
NETWORK	288538
NETWORKS	114459
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INTERFACES	122934
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There are more results than shown above. Click here to view the entire set.

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L2: Entry 2 of 3 File: USPT Jan 23, 2001

DOCUMENT-IDENTIFIER: US 6178462 B1
TITLE: Protocol for using a PCI interface for connecting networks

Abstract Text (1):
A system for coupling a local area network to a wide area network utilizes a PCI (Peripheral Component Interface) bus to couple a PCI interface to a PCI network interface card, which is coupled to the wide area network. The wide area network could be an asynchronous transfer mode network or a high bandwidth ethernet. If the PCI network interface card operates as a PCI master, then the PCI interface will operate as a PCI slave. If the PCI network interface card operates as a PCI slave, then the PCI interface of the invention will operate as a PCI master.

Current US Original Classification (1):
709/249

Current US Cross Reference Classification (1):
709/208

Current US Cross Reference Classification (2):
709/209

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US006178462B1

(12) **United States Patent**
Bass et al.

(10) **Patent No.: US 6,178,462 B1**
(45) **Date of Patent: Jan. 23, 2001**

(54) **PROTOCOL FOR USING A PCI INTERFACE FOR CONNECTING NETWORKS**

(75) Inventors: **Brian M. Bass**; **Dennis Albert Doidge**, both of Apex; **Edward Hau-chun Ku**, Cary; **Scott J. Lemke**, Raleigh; **Joseph M. Rash**, Wake Forest; **Loren Blair Reiss**, Raleigh, all of NC (US)

(73) Assignee: **International Business Machines Corporation**, Armonk, NY (US)

(*) Notice: Under 35 U.S.C. 154(b), the term of this patent shall be extended for 0 days.

(21) Appl. No.: **08/977,230**

(22) Filed: **Nov. 24, 1997**

(51) **Int. Cl.**[7] **G06F 15/16**; G06F 13/00

(52) **U.S. Cl.** **709/249**; 709/208; 709/209; 710/110

(58) **Field of Search** 709/249, 218, 709/236, 300, 250, 208, 209; 710/126, 35, 129, 128, 110

(56) **References Cited**

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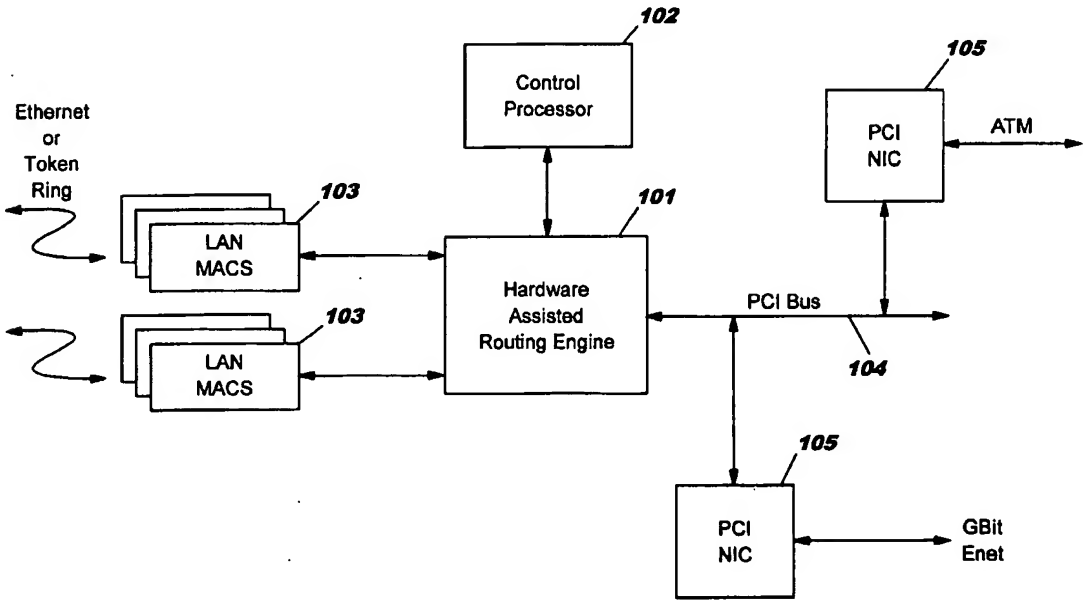
Primary Examiner—Glenton B. Burgess
Assistant Examiner—Quoc-Khanh Le
(74) *Attorney, Agent, or Firm*—John J. Timar; Winstead, Sechrest & Minick

(57) **ABSTRACT**

A system for coupling a local area network to a wide area network utilizes a PCI (Peripheral Component Interface) bus to couple a PCI interface to a PCI network interface card, which is coupled to the wide area network. The wide area network could be an asynchronous transfer mode network or a high bandwidth ethernet. If the PCI network interface card operates as a PCI master, then the PCI interface will operate as a PCI slave. If the PCI network interface card operates as a PCI slave, then the PCI interface of the invention will operate as a PCI master.

31 Claims, 5 Drawing Sheets



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US Patents Full-Text Database
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Derwent World Patents Index
IBM Technical Disclosure Bulletins

Term: L1 and (((NIC) or (network adj1 interface adj1 card)) with peripheral$ with download$)

Display: 10 **Documents in Display Format:** KWIC **Starting with Number** 1

Generate: ○ **Hit List** ◉ **Hit Count** ○ **Side by Side** ○ **Image**

Search Clear Interrupt

Search History

DATE: Thursday, February 17, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=ADJ			
L6	L1 and (((NIC) or (network adj1 interface adj1 card)) with peripheral$ with download$)	1	L6
L5	L1 and (((NIC) or (network adj1 interface adj1 card)) with peripheral$with download$)	0	L5
L4	L1 and (((NIC) or (network adj1 interface adj1 card)) with peripheral$)	82	L4
L3	6141705.pn.	1	L3
L2	L1 and (((NIC) or (network adj1 interface adj1 card)) with peripheral$).ab.	3	L2
L1	709/$.ccls.	17245	L1

END OF SEARCH HISTORY

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